REMARKS

Claim Rejections Under 35 U.S.C. §103

Claims 1, 2, 3, and 7 were rejected under 35 U.S.C. §103(a) as being anticipated over *Chen et al.* (U.S. Patent No. 6,324,602) in view of *Silverbrook* (U.S. Patent Pub. No. 2002/0071104A1). Claims 5, 6, 8 – 12, and 15, 19 were rejected under 35 U.S.C. §103(a) as being anticipated over *Chen et al.*, *Silverbrook* and further in view of *Deneroff et al.* (U.S. Patent No. 6,215,686) and *Mills et al.* (U.S. Patent No. 6,385,688). Applicants respectfully traverse this rejection.

Chen et al. discloses an input/output interface for an integrated circuit device. *Chen et al.* additionally discloses a RAMBUS memory device as applied to a DRAM (column 1, line 66 – col. 2, line 9), a flash memory device, and a DRAM that transfers data on both edges of a clock (column 1, lines 55 – 57). However, *Chen et al.* neither teaches nor suggests a flash memory that has RAMBUS -compatible interconnections and circuitry to provide input and output data on rising and falling edges of a clock as claimed in the present application. The flash memory device mentioned in *Chen et al.* is mentioned only in reference to typical memory devices and no detail is provided as to any flash memory functionality. The DRAM disclosed in *Chen et al.* cannot be equated with a flash memory since they have different bus interconnections, functions, and transistor architecture.

Silverbrook discloses an image sensing apparatus that includes a microcontroller and memory. The memory includes a 4 Mbyte flash memory 70 and DRAM with a RAMBUS interface 81. There is no teaching or suggestion that the flash memory includes, can include, or even a desire to include the RAMBUS interface, as claimed in the present invention. Figure 3 clearly shows and paragraphs 450 and 454 state that the flash memory and the DRAM with the RAMBUS interface are completely separate.

Neither *Chen et al.* nor *Silverbrook* individually teach or suggest the present invention. Even if it were obvious to combine *Chen et al.* with *Silverbrook*, and Applicants maintain that it is not, the combination does not teach or suggest the present invention.

Deneroff et al. discloses a memory system that has switches for controlling data transfer. *Deneroff et al.* neither teaches nor suggests Applicants' invention for a flash memory as claimed in the present application. Therefore, even if it were obvious to combine *Chen et al.* with *Deneroff et al.*, the combination does not disclose Applicants' invention.

Mills et al. discloses an asynchronous interface for a non-volatile memory. *Mills et al.* neither teaches nor suggests the present invention as claimed. Since none of the above-discussed references teach or suggest the present invention, the combination of *Mills et al.* with the above references cannot teach or suggest the present invention.

Double Patenting Rejection

Claims 1 – 6 and 8 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,741,497. Applicants have included a Terminal Disclaimer herewith to address the rejection. In view of the Terminal Disclaimer, Applicants respectfully request reconsideration and withdrawal of the rejection, and allowance of claims 1 – 6 and 8.

CONCLUSION

Applicants respectfully request that the Examiner withdraw his rejection and allow the present claims. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

Date: 9/7/04

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